Amendments to the Specification:

Please replace paragraphs [0006], [0008], [0010], [0016], [0017] and [0025] with the following amended paragraphs:

[0006] FIGs. 1A through 1H are partial cross-sectional views illustrating a first embodiment for formation of a SSOI trench according to the present invention. In FIG. 1A, a substrate **100** having a top surface **105** is illustrated. In a first example, substrate **100** is a monocrystalline (bulk) silicon substrate lightly doped P type (e.g. 1E17 atm/cm^3). In a second example, substrate **100** is a substrate having at least a monocrystalline silicon layer extending to top surface **105**. A first dielectric layer **110** having a top surface **115** is formed on top surface **105** of substrate **100**. A second dielectric layer **120** is formed on a top surface **115** of second dielectric layer **110**. In one example, first dielectric layer **110** is a thermal oxide having a thickness of about 40 to 100 [[Ã]] Å and second dielectric layer **120** is silicon nitride having a thickness of about 900 to 1200 [[Ã]] Å.

[0008] In FIG. 1C, patterned photoresist layer **125** of FIG. 1B is removed and an N type ion implantation performed using the now patterned first and second dielectric layers **110** and **120** as ion implantation masks in order to form N-doped region **140A** and **140B** in substrate **100**. In one example, arsenic (As), phosphorus (P), antimony (Sb) ions or combinations thereof are implanted at energies of about 1 Kev to 10Kev and doses of about 1E14 atm/cm^2 to 1E16 atm/cm^2. However, any species that dopes silicon N type may be used. A rapid thermal anneal (RTA) of 950°C to 1050°C is performed in order to activate the species in N-doped regions **140A** and **140B**. N-doped regions **140A** and **140B** extend a distance D1 from top surface **105** of

substrate **100** into the substrate. In one example, D1 is about 300 to 1000 [[Ā]] Å. N-doped regions **140A** and **140B** may also be formed by other dopant techniques such as solid state diffusion from a doping layer or a vapor.

[0010] In FIG. 1E, a first dielectric layer **150** is formed on a top surface **155** of epitaxial layer **145** and a second dielectric layer **160** is formed on a top surface **165** of the first dielectric layer. In one example, first dielectric layer **150** is a thermal oxide having a thickness of about 40 to 100 [[Ā]] Å and second dielectric layer **160** is silicon nitride having a thickness of about 900 to 1200 [[Ā]] Å.

[0016] FIG. 2A is similar to FIG. 1C. In FIG. 2A, the patterned first and second dielectric layers **110** and **120** are ion implantation masks for defining N-doped regions **140C** and **140D** in substrate **100**. In one example, As, P, Sb ions or combinations thereof are implanted at energies of about 150 Kev to 400 Kev and doses of about 1E14 atm/cm^2 to 1E16 atm/cm^2. However, any species that dopes silicon N type may be used. A rapid thermal anneal (RTA) of 950°C to 1050°C is performed in order to activate the species in N-doped regions **140C** and **140D**. N-doped regions **140C** and **140D** are buried a distance D2 from top surface **105** of substrate **100** into the substrate and have a vertical depth D3. In one example, D2 is about 750 to 1250 [[Ā]] Å and D3 is about 300 to 1000 [[Ā]] Å.

[0017] FIG. 2B is similar to FIG. 1E. In FIG. 2B, first and second dielectric layers **110** and **120** of FIG. 2A are removed and first dielectric layer **150** is formed on top surface **105** of substrate **100** and second dielectric layer **160** is formed on top surface **165** of the first dielectric

layer. In one example, first dielectric layer **150** is a thermal oxide having a thickness of about 40 to 100 [[Ã]] Å and second dielectric layer **160** is silicon nitride having a thickness of about 900 to 1200 [[Ã]] Å.

[0025] FIG. 5B is a partial cross-sectional view of an optional completed SSOI isolation structure according to the present invention. In FIG. 5B, a completed SSOI isolation **185B** is illustrated after removal of first and second dielectric layers **155** and **160** (see FIG. 3E). The only difference between SSOI isolation **185A** of FIG. 5A and SSOI isolation **185B** is the presence of a liner **235** between first insulator **210**, second insulator **215** and third insulator **220** and silicon substrate **100** and epitaxial layer **145**. Liner **235** is formed prior to the processes illustrated in FIG. 3A or 4A and described *supra*. In one example, liner **235** comprised of a first layer of rapid thermal oxidation (RTO) oxide formed on exposed silicon surfaces of the unfilled SSOI trenched coated with a conformal plasma-enhanced CVD (PECVD) silicon nitride layer. In one example, the RTO oxide is about 100 to 150 [[Ã]] Å thick and the PECVD silicon nitride layer is about 50 to 80 [[Ã]] Å thick.